REMARKS

Reconsideration of the present application is respectfully requested. Claims 5 and 6 have been amended. No claims have been canceled or added.

Clams 17-26 stand allowed. Claims 3, 4, 6-12, 15, and 16 stand objected to as being dependent on a rejected base claim but were deemed to be otherwise allowable. Claims 1 and 13 stand rejected under 35 U.S.C. § 102(a) based on European Patent application no. EP 0797149 of Mohamed et al. ("Mohamed"). Claims 1, 2, 5, 13 and 14 stand rejected under 35 U.S.C. § 102(e) based on U.S. Patent no. 6,564,311 of Kakeda et al. ("Kakeda"). Claims 1-26 are further rejected for non-statutory obviousness-type double patenting based on the parent patent, U.S. Patent no. 6,728,858.

The above claim amendments are made only to correct a minor informality. The amendment is not made in response to the rejections or to comply with any statutory requirement of patentability, since no such amendments are believed to be necessary.

Double Patenting Rejection

Submitted with this response is a terminal disclaimer relating to U.S. Patent no. 6,728,858, which Applicants believe overcome the non-statutory obviousness-type double patenting rejection.

Prior Art Rejections

Applicants appreciate the allowance of claims 17-26 and the indicated allowability of dependent claims 3, 4, 6-12, 15, and 16. However, Applicants respectfully traverse the prior art rejections of claims 1, 2, 5, 13 and 14. Neither

Mohamed nor Kakeda discloses or suggests the present invention, as set forth in any of Applicants' claims.

Each of the rejected independent claims recites (among other things) a plurality of logical processors. Claim 1, for example, is directed to a technique which determines whether a plurality of logical processors can share an address translation.

It is important to recognize the difference between a process and a processor. A process is a sequence of steps or operations. A processor is an element which executes one or more processes. Likewise a "logical processor" is a logical element which executes one or more processes.

Mohamed and Kakeda both disclose techniques that allow TLB entries to be shared by multiple processes running on a single processor (e.g., a CPU). Neither Mohamed nor Kakeda discloses or suggests the use of a plurality of logical processors, much less a technique that determines whether TLB entries can be shared by a plurality of logical processors. For at least this reason, therefore, the present invention is not anticipated by, or obvious in view of, the cited art.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 2/2/06

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(Signature of person mailing correspondence)